Power Quality Improvement in Modular Multilevel Inverter Using for Different Multicarrier PWM

Thenmalar Kaliannan, Johny Renoald Albert, D. Muhamadha Begam, and P. Madhumathi

Abstract — Pulse width modulation (PWM) is a powerful technique employed in analog circuit convert with a microprocessor based digital output. Besides, Pseudo Random Multi Carrier (PRMC) involves in two random PWM strategies to minimize the harmonic order for 9-level cascaded multilevel H-bridge (CHB) inverter and 9-level Modular Multilevel inverter are introduced. The design mainly focuses on the (Pulse Width Modulation) PWM method, in which two nearest voltage levels are approached in estimated output voltage prediction based on the Partial swarm optimization (PSO) algorithm, and it conveys a random variation in the pulse position of output by Pseudo Random Multi Carrier- Pulse Width Modulation (PRMC-PWM). The CHB and the Modular inverters generate low distortion output by using PMRC. The simulation and prototype circuit are developed for the nine level output using sixteen switches and ten with Resistive-Inductive (R-L) load variation condition. The power quality is improved in CHB and Modular inverter (MoI) with minimized harmonics in various modulation index (MI) as varied from 0.1 up to 0.8. The circuit is designed by using a Field Programmable Gate Array (FPGA), Implementing a PSO algorithm for both CHB, and MoI are proposed. The comparisons of results are verified with lower order harmonics and find the best switching angle across the MLI switches. Modular inverter furthermore investigates with PRMC, Random Nearest level (RNL) modulation scheme are presented, and the proposed circuit is along with the respective degree of the output voltage were synthesized in non-linear load by the development of reactive power across a motor load.

Index Terms — Cascaded H-bridge (CHB), Modular Inverter (MOI) Total Harmonics Distortion (THD), Particle Swarm Optimization (PSO), Field Programmable Gate Arrays (FPGA), Pseudo Random Multi Carrier Pulse Width Modulation (PRMC-PWM).

I. INTRODUCTION

A multilevel inverter has several advantages for utility distribution, linear and non-linear load conditions, i.e., linear load like as R load, and non-linear load like as R-L, RLE load. This is normally operating an AC or DC source applied in a commercial and most of the usage in a residential application. The MLI operates in an input of the DC voltage source, which is used for high or medium or low level switching frequency PWM scheme to generate the multilevel output. There are three main kinds of multilevel inverters in basic MLI topology, Diode-Clamped (D-C), Capacitor-Clamped (C-C), and Cascaded-H Bridge (CHB) topology. However, the series connection of several basic H-bridge inverters is widely utilized in reactive power improvement [1], renewable energy power generation [2], energy storage [3], and AC drive [4], [5]. Cascade inverter results in staircase output, here the

symmetric cascade multilevel inverters topologies are proposed. This is the value of dc voltage magnitude unequal. This type of inverters is characterized by the fact that the potential difference across dc-link capacitors is unequal.

In asymmetric inverter, the number of switches can be different multilevel inverter circuit configuration, and it is unequal or changes in dynamically the input, but symmetrical methods are equal magnitude. Which is not applicable for non-linear load condition, due to lower order harmonics and control complexity of the circuit is enormous. The cascade multilevel converters are consisting of a different modulation scheme with unequal DC voltage applied in MLI circuit, the different DC voltage sources convert with the various modulation techniques presented [6], [7]. Essakiappan et al. [8] have propounded, the converters are reduced the bulky semiconductors enhanced in reliability since more filters, and cost of the inverter employed in CHB-MLI. In a multicarrier modulation scheme is an employee to generate the gating signals for the individual switches. That is used to increasing the output voltage with unbalanced dc-link capacitor.

Therefore, the random PWM strategies along with three main modulations are: Randomized Carrier-Based (RCB), Randomized Space Vector (RSV), and Dithered Sigma-Delta (DSD). In last 40 years, RPW strategy have been applied for DC-AC converters [9]-[12], random multi-carrier inverter [13]-[14], and filter active converter circuits [15]. In proposed system is reduced cost of the filter. K.K. Gupta et al. [16] have proposed by Random Nearest Level (RNL) Strategy of multilevel-CHB inverter 25 switches, 2 random combinations of 5-level cascaded multilevel inverter, based on two random nearest level (RNL) strategies to reduce harmonic spikes of multilevel CHB inverter are presented, and the discrete Random Nearest Level (DRNL), Continuous Random Nearest Level (CRNL) are randomly varied the pulse position. To compare with a deterministic nearest level modulation (DNLM) strategy, the initially proposed strategy is provided two discrete pulse positions selected with a random bit. The most significant recent in advanced power electronics is reduced switching count modular inverter by utilizing modified pseudo random multi carrier proposed. It consists of 8 switches, 9 levels, and 2 random combinations of two RNL voltage levels approximate output voltage predicated by using PSO algorithm. It randomly varies the pulse position of output voltage by selecting a random output instant of two RNL level. The optimization of control algorithm using PSO that is used to find optimum switching angle, and also minimized THD level using FFT analysis of the output voltage waveforms verified. Pseudorandom multi

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Thenmalar Kaliannan
Johny Renoald Albert
(e-mail: jorennoee@gmail.com)

D. Muhamadha Begam
P. Madhumathi

carrier (PRMC) involves two random PWM strategies to reduce the harmonic order for 9-level CHB, Modular Inverter (MoI) is proposed when it is analysis the THD and compensating reactive power in series (R-L load) Asynchronous machine-capacitor start motor are verified.

The strategy is to utilize random pulse width (RPW) strategy to acquire a spread spectrum with reduced harmonic spikes. The multilevel inverter does not produce any power, the energy is provided by the DC source, it is widely utilized in industrial and domestic applications. The CHB-MoI MLI is used to increase the reactive power in R-L load by using PRMC approach. This technique can be implemented in MATLAB/ Simulink function of varying switching instants randomly without any extra filter component.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

The CHB is also known as one type of traditional multi-cell converter. It made up of series connected CHB. In this structure, each H-bridge is supplied by an isolated DC source of indistinguishable value, i.e., Batteries, fuel cells, or ultra-capacitors are used as isolated the dc sources [17]-[21]. DC source is fed with connected in a series on AC circuit. Output voltage is attained by countable voltages produced by each H Bridge connected to same form of CHB circuit. Each cell creates nine multilevel voltages. It can obtain positive, zero and negative by linking DC source to AC output from beginning to end modulation arrangements of sixteen switches. The CHB is presented sixteen switch and 4-DC sources. The sixteen switches have been approved in the appearance of four H-bridges with each other. By rotating on S1-S4, S5-S8, S9-S12, or S13-S16, switch the related voltage source is reflected as a positive output load appearance. Similarly, by trigger on the switches S2-S3, S6-S7, S10-S11 or S14-S15 corresponding voltage is reflected as negative output at the load.

III. PROPOSED MODULAR INVERTER (MOI) OR REDUCED MULTILEVEL CONNECTION (RMC)

In the conventional and trinary configuration, the changes are realized in the control circuit to achieve 9 levels but in the proposed technique only eight switches are required to develop the power circuit and PRMC is adopted for obtaining 9 level. A single-phase RMC topology is shown in Fig.1. The modes of operation are presented in section III, A. From the operating modes, the polarity generation switches (T1, T2) for a positive half cycle and (T3, T4) for a negative half cycle are in ON condition and the level generation switches (S1–S4) is controlled to attain 9 levels. The dc input voltages are given from the PV array. Let the inputs of array voltage can be split-up into four stage PV1, PV2, PV3, and PV4. First level is generated by operating Vdc1 alone while the other dc voltage sources are inoperative. Correspondingly, the 9 levels are obtained by turning ON and OFF the switches. The input dc sources fed from PV array are in the ratio of 1:1:1:1.

A. Operating Modes of RMC

The proposed 9-level RMC inverter has different modes of operation. In the positive half cycle the output voltages obtained are +1Vdc, +2Vdc, +3Vdc, +4Vdc. The output

voltages obtained for the negative half cycles are -1Vdc, -2Vdc, -3Vdc, -4Vdc.

1) Stage-I: To generate an output voltage level of $V_o = +V_{dc}$, S1 is turned ON at the positive half cycle. S1, T1, and T2 are turned on and the voltage applied to the load terminals is +Vdc.

2) Stage-II: To generate an output voltage level of $V_o = +2V_{dc}$, S1, S2 is turned ON at the positive half cycle. S1, S2, T1, and T2 are turned on and the voltage applied to the load terminals is +2Vdc.

Fig. 1. Nine-level RMC topology.

3) Stage-III: To generate an output voltage level of $V_o = +3V_{dc}$, S1, S2, and S3 is turned ON at the positive half cycle. S1, S2, S3, T1, and T2 are turned on and the voltage applied to the load terminals is +3Vdc.

4) Stage-IV: To generate an output voltage level of $V_o = +4V_{dc}$, both S1, S2, S3 & S4 are turned ON at the positive half cycle. S1, S2, S3, S4, T1, and T2 are turned on and the voltage applied to the load terminals is +4Vdc. For generating the negative levels, the Switches from Stage I to IV are repeated by triggering T3 and T4 switches.

B. PWM Methods of Multi Carrier Based Technique

The core objective of the modulation scheme of the multilevel inverter is to synthesize the output voltage as nearly as possible to the sinusoidal waveform. Many modulation methodologies have been applied for the reduction of harmonics and the improvement of power efficiency. In multilevel inverters with high switching frequencies, modulation methods are used for several switches for power semiconductors in one cycle of the fundamental output voltage presented [22]-[28]. The switching status of the inverter leg is determined by a comparison of the modulating signal providing the voltage reference information, and the carrier signal providing MLI switching time information is intended for higher power applications. Because of the larger switching loss, and the semiconductor switching technology has been inherent in operating speed limits.

These are classified into two types:

1. Level Shift.
2. Phase Shift.

To recognize the maximum power factor for a PWM controlled by MLI's are proposed. It investigates the different forms of multilevel triangle-sine wave PWM and shifting an entire waveform, up or down. It is provided for both high and low voltage levels.

The multi carrier signals takes a maximum time period value of each carrier waveforms are set. The values of the outputs are set according to the configuration of the carrier waves. The output signals of the comparator will be sent to each semiconductor switches. In order to achieve a stepped multilevel output waveform within the lower distortion suggested carrier level change of $180^\circ/m$ signal is applied to MLI switch. However, this is not suitable for produced a phase voltage. Where 'n' is the number of full bridge inverters in a multilevel phase leg.

$$\theta = 180^\circ / (N - 1) \quad (1)$$

Three alternatives exist modulation PWM strategies with dissimilar phase relationships for the level-shifted (N-1) carriers presented [29]-[32].

- Phase Disposition (PD) PWM.
- Phase Opposition Disposition (POD) PWM.
- Alternative Phase Opposition Disposition (APOD) PWM.

In PRMC-PWM is all triangular carriers signal attempt equal frequency, and equal maximum amplitude. But two adjacent carrier waves are a phase shift between potential differences. For 'm' Voltage levels (m-1) carrier signals, and the phase shifted with an angle of $\theta = (360^\circ/m-1)$ is required. The switching signals are generated with a suitable evaluation of a carrier and modulating signal wave. However, since the carrier signals are not synchronized, but the output line to line voltage is reduce dv/dts stress across the switches.

C. Proposed Strategy

The arrangement of a MLI is proposed to reduce harmonic distortion for each multilevel level. MLI can generate three different voltage outputs (+Vdc, 0, and -Vdc) by converting the DC to AC output. Inverter provides two discrete pulse positions, and first one is selected by a random bit. Where, pulse positions randomly vary the output voltage by using two RNL level. A maximum degree of freedom can be achieved in strategy with lower harmonic spikes, but higher commutation frequency is compared with the CHB, and MoI-MLI strategy. AC outputs of each separate full-bridge and MOI number of levels are connected in series such that the synthesized reference voltage, the sum of the inverter outputs, and also the output phase voltage levels 'm' is an inverter described by (N-1). This can be generated by two random bit sequences. Where, 's' is the number of various origins of DC source.

Fig. 2. Two output Sequence VAL and VAU.

a. Output sequence from VAL to VAU when a random bit is "0".

b. Output sequence from VAU to VAL when a random bit is "1".

There are 2 fundamental output sequences of RNL modulation. Throughout this case, the various types of multilevel sine-triangle PWM are explored, and the lower level followed by the upper level has become single sequence of the output. Another method is the reverse sequence, i.e., the upper level output at the beginning of the sampling cycle (8.8 e-06 s), and then the random carrier signal verifies the lower level output. The random bit "0" or "1" to pick the output sequence as seen in the Fig. 2. Where leg A is seen, the output series of two RNL begins from the lower level VAL to the upper level VAU. Whether the random bit is "0," (or) if not, the output is the opposite sequence. The resultant phase voltage is synthesized by adding the voltages that the various cells produce. By using the four different voltages from the DC (or) PV input for each single-phase H- bridge, and MoI inverter are generates staircase output in a 9-level. The MLI uses pseudo random multi carrier PWM/ RNL modulation to decrease the switching count in the MOI inverter. The optimization of control algorithm using PSO, which is the voltage level increase to find optimum switching angle in a conventional (MoI) MLI.

Fig. 3. PRCM-PWM with pulse position by a random interval.

Where a random interval (δ) delays the pulse position ' Δt '. The scale will differ continuously from 0 to T_s , and the highest degree of freedom is obtained by the PRCR-PWM strategy. If the maximum interval value is set as ' T_s ' as seen in Fig.3. After that, the location of the pulse is postponed avoiding overlapping of the pulse pattern during the next sampling cycle. The part of voltage pulse pattern, which is throughout the sampling that should be shifted into the beginning of the present sampling period. In these strategies 16 switches-CHB (or) 4 switch-MoI two random combinations of nearby voltage levels into approximate output voltage are easily predicated. It is developed by MATLAB code for synthesizing in a level shifted PWM gating signals passing through the MOSFET switch. The

main concepts of CHB-MLI to reduce the power switch count across the load variation (RL load) along with the respective degree of output voltage level were synthesized for effectiveness of the proposed method.

IV. IMPLEMENTATION OF PRMC WITH TWO-RNL METHOD

A PRMC-PWM scheme for different multilevel converters to the elimination of lower-level harmonics. The optimized PRMC strategy provides improved performance over traditional random PWM scheme, it can ideal RPWM technique to represent results in power spectra of MLI voltage. The proposed MLI is present a fundamental frequency harmonic, and continuous noise spectral is also minimized. In this method of higher harmonics over the entire frequency range is free. In practicality, such an ideal FFT spectrum is possible with technical limitations. It is imposed on the sufficient switching patterns and investigates an existing topology.

Hence, a new random carrier technique presents in CHB inverter for harmonic minimization [33]. In PRMC approach should be different random carrier sequences applied within a minimum period. The modulation is verified under the over current pulse shifting technique at the beginning of the switching period. This approach is applied only in bridge circuit topology because the random interval is possible in every CHB circuit. The Pseudo Random Carrier PWM technique is similar to conventional Sinusoidal-PWM, while it uses two different triangular carriers. One is required frequency, and another one is 180° Phase shifted. The selection of the signals among the RNL carriers is done by a random bit generated. That is '1' output carrier (basic) selected in each carrier 2(180° shifted). The selection is done forever carrier cycle, and the selected carrier is compared with the reference sinusoidal waveform. The PRMC scheme is most commonly used for the random triangular frequency generation. A simple concept of randomly modulated carrier PWM is illustrated in Fig. 4. Besides, the PRMC involves in two random PWM strategy reduced the harmonics pikes for 9- level CHB/MoI inverter are developed.

Fig. 4. Pseudo Random Carrier PWM Signal Generations.

PRMC involves in 2-random pulse strategies is reduce the harmonic order proposed. The sine-triangle signal using carrier waveform is applied in the inverter switch. Therefore, the modulating signal generations are investigated with the random comparator model, and it is produced with a modulation index value. THD is a ratio of the sum of power in all harmonic, which is divided by fundamental frequency, the fundamental frequency is to compare the system output power frequency [34]-[37].

$$THD = \frac{\text{Harmonic Power}}{\text{Fundamental harmonic power}} \quad (2)$$

The modulation index is defined as the correlation between the information of the amplitude signal and carrier of the amplitude signal shown in (3).

$$\text{Modulation Index (MI)} = \frac{V_{\text{ref}}}{V_{\text{carrier}}} \quad (3)$$

To reduce the THD of sine-triangle PWM inverter using carrier waves are generated by a random pattern of binary values. The shape of a carrier signal is varied under the instantaneous binary values. An example of the modulating level shifted random carrier is applied in the inverter switch, the random PWM output is developed by PRMC signal, it is two random PWM strategies to reduce the harmonic spikes across the nonlinear load, when it is minimized the lower order THD is compensating in reactive power to the series R-L load (Asynchronous machine-capacitor start).

The method is used to RPW modulation strategy attain a spread spectrum analysis with minimized the over current across the switches.

V. SIMULATION IMPLEMENTATION OF CARRIER BASED TRIGGERING

A random triggering based Pseudo random multicarrier PWM (PRMC-PWM) modulation is the main functions of power conversion perform with improved power quality, and reduces THD level. Under the assumption of the signal is not necessary periodical triggering, which is used as random modulation to be obtained in the measurements of the signal is randomly chosen by a clock generator. The optimized PRPWM strategy provides enhanced performance of over traditional random pulse schemes are developed in carrier based triggering. This triggering is based on the clock and some logic operator within the time delay operation as shown in Fig. 5. An ideal RPWM technique described in the power spectra of inverter voltage is containing a fixed frequency harmonic. It is further continuous in spectrum analysis approach. Which is free of lower harmonics in the entire frequency ranges up to the nth level. The distinct ability to estimate frequency high level triggering depends on the time digital converter devices, it is previously used in random equivalent modulation scheme in CHB inverter. In this method is used XOR gate is applied in multiple measurements in PWM approach. In this investigation is estimated the output in each switch operates in a random triggering scheme. The switch is operated in positive and negative signal frequency domain in each quadrant.

Fig. 5. Pseudo random carrier based triggering circuit.

The proposed inverters are generated by using multicarrier modulation in first-order equations. In switching, the element of conventional full-bridge and MoI inverter are connected to the centre tap of DC power supply. The proper switching control of the auxiliary switch of MoI can generate a half-level DC supply voltage. It has four switches that need to turn ON. Similarly, for another CHB circuit eight switches output operates the random triggering circuit for both positive (or) negative to be tuned on NOT gate. This proposed module is capable of producing nine level output voltage, and the gating signals for the inverters are generated by using Pseudo Random technique output. In PSO, that is the voltage of two RNL level increases to find optimum switching angle in a proposed 9-level inverter.

VI. IMPLEMENTATION OF PARTIAL SWAM OPTIMIZATION

Partial Swarm Optimization (PSO) is a stochastic optimization technique. A population based search method is also called a position of particle optimization, and swarm of the particles as a searching agent in PSO approach is a robust evolutionary optimization method based on the movement, and the intelligence of swarms are discussed [38], [39]. PSO is to find the minimum value for the function in each particle for the search fly space. It is evaluated in a velocity equation, which is dynamically tuned according to its own flying experience. Its companion flying experience represents in Ith particle as $X_i = (x_{i1}, x_{i2} \dots x_{iD})$. In the Ith particle, the best prior location of the fitness value evaluated is registered, and expressed as $P_i = (p_{i1}, p_{i2} \dots p_{iD})$. The best particle index of all the particles in the 'I' population, defined by the symbol (g). The rate of the position shift (velocity) for particle 'I' is represented as $V_i = (v_{i1}, v_{i2} \dots v_{iD})$. According to the location, the particles are manipulated to the following:

$$V_{id} = w * v_{id} + c_1 * \text{rand}() * (p_{id} - x_{id}) + c_2 * \text{Rand}() * (p_{gd} - x_{id}) \quad (4)$$

$$S_{id} = S_{id} + V_{id} \quad (5)$$

There are two positive constants C_1 , C_2 , and two random functions as $[0, 1]$. 'W' is inertia weight. It has been characterized by the significance of temperature parameter simulated. The equation (4) is the earlier velocity of the particles. Second is the "cognition" part, representing the exploiting own swarm experience. Where C_1 is an individual factor and "social" pan representing as shared information, and C_1 , C_2 is the societal factors cooperation among the optimization particles.

Each particle tries to modify the own position 'X' based on the following formula:

$$X(t+1) = X(t) + V(t+1) \quad (6)$$

$$V(t+1) = wV(t) + c_1 \times \text{rand}() \times (X_{pbest} - X(t)) + c_2 \times \text{rand}() \times (X_{gbest} - X(t)) \quad (7)$$

$V(t)$	Particle at time of velocity (t)
$X(t)$	Time based on particle position (t)
W	Inertia weight(w)
c_1, c_2	accelerating factor (or) learning factor
rand	Random number between 0 and 1 uniformly distribution
X_{pbest}	Best position of particle's
X_{gbest}	Best position of Global

The PSO algorithm pseudo code steps are follows:

Input: Position and velocity of each Particle in randomly initialization: $X_i(0)$ and $V_i(0)$.

Output: Global minimum approximate position X as shown in Fig. 6.

Step 1: while terminating condition is not reached.

Step 2: for $i = 1$, Number of particles.

Step 3: Fitness function calculation.

Step 4: Update particles position for X_{pbest} & X_{gbest} (Personal best and Global best).

Step 5: Update the particle velocity equation (6).

Step 6: Update the particle position equation (7).

Step 7: end for loop.

Step 8: end while loop.

Fig. 6. Flowchart for concept of PSO.

VII. SIMULATION RESULT AND DISCUSSION

The simulation model has been developed by using the MATLAB/Simulink program. Gating signals for inverters are produced using a multicarrier modulation approach. The CHB circuit was simulated with R-L load output as seen in Fig. 7(a). Pulse generation of PRMC circuit is designed by using Matlab/2019a. The generated voltage spectrum for nine level inverter topology simulation results is verified, and MOI inverter requires the least number of switches, and sinusoidal output are generated for high quality voltage with minimum

harmonics. The switching pulses and best switching angle are generated for each MLI switches based on a PSO algorithm. Similarly, it generates a pulse with Magnitude '1' indicates that the switch is 'ON' and the magnitude '0' indicates that the switch is 'OFF'. An output voltage waveform is obtained by summing of both the cells connected in series. The PSO approach is a minimum computational time within the best optimum values in Table I.

Fig.7(a). Simulink Output waveform of nine levels CHB-MLI.

TABLE I: THD ANALYSIS OF MOI USING RL-LOAD

Modulation Index	Optimization Turning	THD% RL load	Optimum Switching angle with modulation index (MI)
0.8	Partial Swam Optimization (PSO)	7.44	$\alpha_1 = 18.95, \alpha_2 = 21.50$
0.7		12.74	$\alpha_3 = 33.91, \text{ and } \alpha_4 = 53.91$
0.6		3.35	$\alpha_1 = 28.05, \alpha_2 = 19.21$
0.5		10.12	$\alpha_3 = \mathbf{31.54}, \text{ and } \alpha_4 = 43.91$
0.4		11.50	$(\text{MI} = 0.63)$
0.3		3.83	$\alpha_1 = 5.37, \alpha_2 = 29.21$
			$\alpha_3 = 43.54, \text{ and } \alpha_4 = 73.91$
			$(\text{MI} = 0.72)$

The measurement of different input and output powers are evaluated within the fundamental frequency 50 Hz. The output voltage obtained across each basic unit of the proposed inverter topology during the symmetric operation, the total voltage stress on switches is calculated.

Fig. 7 (b). Shows the output of the MoI inverter. In MATLAB-Simulink, existing MLI topology with various experts compared THD analysis as shown in Table II. The FFT analyses of the output voltage waveforms are accomplished by the corresponding THD values obtained. The Sampling time is 8.8×10^{-6} s to calculate the samples per cycle range 2273 respectively. The basic frequency of sinusoidal reference waveform is compared to high frequency carrier waveforms having the same amplitude with a peak value of 240 V and an RMS value of 140.69 V. Fig. 8 (a and b) presents the minimum THD of the MOI as 3.35%. The MLI's can reduce total harmonic distortion (THD) for both full load and half load conditions. But the proposed MoI, RL load connected motor such as a capacitor-start, or capacitor run is including a dual run electrical capacitor that alters the current in one or more windings in a single phase induction motor as shown in Fig. 9. This is creating the rotating magnetic field with the respective modulation scheme. It reduces the power switch count across the load variation (RL load) along with the respective degree of various RL output parameters are confirmed in a nonlinear load. The rotor did

not require any current to adjust the applied torque in the start motors of the capacitor.

Fig.7 (b). Simulink Output waveform of nine levels MOI.

(a)

(b)

Fig. 8Total Harmonic Distortion of: (a) CHB using FFT analysis, (b) MOI using FFT analysis.

The single phase induction motor uses a capacitor in the auxiliary winding circuit, which creates a larger phase change between the main current and the auxiliary winding of the system. In this modulation, technique capacitor starts motor is generated in a main winding current I_a (0-40) p.u, Auxiliary winding current I_b (0-10) p.u, Voltage capacitor V_c (0-200) V, Electromagnetic torque T_e (0-20) N*m, and Rotor speed (0-1000) rpm, respectively.

Fig. 9. RL load (Asynchronous machine-Capacitor start).

VIII. HARDWARE RESULT AND DISCUSSION

The hardware results are obtained from a proposed nine level MOI, which consists of components such that diode, capacitor, battery, FPGA 3A kit, and switches. To show the feasibility of the inverter topology hardware setup is shown in Fig. 10. The voltage levels from DC source convert to AC output power. The FPGA board has generated the pulses to each inverter switch. It can produce the output of 220 V the load current aspects RMS value is 1.5 amps. The H-bridge and each comprised cells absorb the input in three different voltages zero, DC (+ve), and DC (-ve) voltages. By compare the carrier signal with reference waves are provided the switching pattern is experimentally obtained in the modulation index 0.6. THD is finding out for both half load and full load conditions with the improvement of reactive power in non-linear load. Fig. 11 (a and b) shows the THD of the CHB and MOI. The obtained experimental THD is 13.9 and 2.90%. For the 9-level inverter, reactive power increases nearly 30 VAR into 65 VAR are obtained in R-L load as shown in Fig. 12. However, the increases among that voltage value in full load condition are increased by 220 V using for multicarrier PWM. However, the harmonics is decreased in RL load due to the absence of filter mechanism. Thereby providing the compact of power conversions is applied in changes of impedance value across the load. The experimental setup of a multilevel inverter with RL load (Asynchronous machine – Capacitor Start), and the output is measured from digital CRO. To get the constant output voltage waveform obtained from Digital CRO of the proposed inverter, and it is connected in channel 1. The gating signals are generated from Xilinx Spartan 3AN series FPGA controller kit. The driver circuit is used to amplify the PWM signals based nine level MOI is to be designed and implemented to produce multilevel output of desired magnitude and frequency. The PSO algorithm is used in FPGA for producing optimum switching angle for MOSFET (IRF 840) switches for producing required AC output voltage with minimized THD level. The reactive power will be enhanced from a different type of operational non-linear load conditions. The PSO tuned optimum switching value is 31.5°.

Fig. 10. Proposed FPGA assists MoI photography view.

(a)

(b)

Fig. 11. Experimental THD of: (a) MOI, (b) CHB.

The nine level inverter gives minimum THD value of 2.9% in the bandwidth of spectrum varying from 1 kHz to 4.9 kHz for half load and full load condition as shown in Fig.12. Table II shows the main concepts of MOI with reduced power switch count across the load variation (RL load) along with the respective degree of output voltage level were synthesized minimized THD level.

Fig. 12. THD spectrum analysis.

TABLE II: COMPARISON RESULTS WITH FULL LOAD AND HALF LOAD
CONDITION

CHB Simulation and Experimental THD			LOAD
Load (THD %)	Vrms (Full load/Half load)	Frequency (Hz)	
10.46%	240v	50Hz	RL
3.3%	140v	50Hz	RL
MOI Simulation and Experimental THD			
Load (THD %)	Vrms (Full load/Half load)	Frequency (Hz)	LOAD
2.90%	230v	50Hz	RL
12.9%	110v	50Hz	Induction Motor
2.96%	220v	50Hz	Induction Motor

REFERENCES

- [1] Adrian V., Chang J. S., Gwee B.-H., (2010). A randomized wrapped-around pulse position modulation scheme for DC-DC converters IEEE Trans. Circuits Syst. I, Reg. Papers., 57(9): 2320–2333.
- [2] A.A. Valdez-Fernandez, P. R. Martinez-Rodriguez, G. Escobar, C. A. Limones- Pozos and J. M. Sosa, (2013) A Model-Based Controller for the Cascade H-Bridge Multilevel Converter Used as a Shunt Active Filter. IEEE Transactions on Industrial Electronics, 60(11): 5019-5028.
- [3] Anant Kumar Verma, Gagan Singh, (2014), "A Distinct Pseudo Random Carrier Modulation Approach for a Boost Converter, IEEE explore, 970-974.
- [4] Ashraf Ahmed, Mohana Sundar Manoharan, Joung-Hu Park, (2019) An efficient Single Sourced Asymmetrical Cascaded Multilevel Inverter with Reduced Leakage Current Suitable for Single-Stage PV Systems, IEEE Transactions on Energy Conversion, 34(1): 211-220.
- [5] Belwin Edward J, Gowri Shankar. J (2018), Design and implementation of 15- level asymmetric cascade H-bridge multilevel inverter', Journal of Electrical Engineering, 17(2): 396-404.
- [6] Chariag D., Sbata L. (2020) Implementation of different randomized PWM schemes using Atmega328p microcontroller for EMI reduction in boost converter. Electr Eng 102: 1063–1071. <https://doi.org/10.1007/s00202-020-00934-7>.
- [7] Charles I. Odeh, Damian B.N. Nnadi., et al (2013): 'Single-phase 9-level hybridized cascaded multilevel inverter', IET Power Electron., 6(3): 468-477.
- [8] Essakiappan S., Krishnamoorthy H. S., Enjeti P., et al (2015) Multilevel medium-frequency link inverter for utility scale photovoltaic integration, IEEE Trans. Power Electron., 30(7): 3674–3684.
- [9] F. Khoucha, S. M. Lagoun, K. Marouani, A. Kheloui and M. E. H. Benbouzid, (2010) Hybrid Cascaded H-Bridge Multilevel-Inverter Induction-Motor-Drive Direct Torque Control for Automotive Applications. IEEE Transactions on Industrial Electronics, 57(3): 892-899.
- [10] Johny Renoald Albert and Dishore Shunmugam Vanaja, (2020), 'Solar Energy Assessment in Various Regions of Indian Sub-continent, Book chapter (solar cell) in tech open, pp. 1-15. DOI: 10.5772/intechopen.95118.
- [11] Albert, J.R. and Stonier, A.A. (2020), Design and development of symmetrical super-liftDC-AC converter using firefly algorithm for solar-photovoltaic applications. IET Circuits Devices Syst., 14(3): pp.261-269. <https://doi.org/10.1049/iet-cds.2018.5292>.
- [12] Shunmugam Vanaja, D. Albert, JR, Stonier, AA. An Experimental Investigation on solar PV fed modular STATCOM in WECS using Intelligent controller. Int Trans Electr Energy Syst. 2021; e12845. <https://doi.org/10.1002/2050-7038.12845>.
- [13] Kumar A. R. and Thangavelusamy, D. (2019) A modified nearest level modulation scheme for symmetric and asymmetric configurations of cascaded H-bridge inverter, The International Journal of Electrical Engineering & Education. 1-16. doi: 10.1177/0020720919858844.
- [14] A. Johny Renoald, M. S. Keerthana (2016) 'Design and Implementation of Super-Lift Multilevel Inverter using Renewable Photovoltaic Energy for AC Module Application, International Journal of Science Technology & Engineering, 2(11), pp.617-624.
- [15] Krishna Kumar Gupta and Shailendra Jain, (2014), A Novel Multilevel Inverter Based on Switched DC Sources, IEEE Transactions on Industrial Electronics, 61(7): 3269-3278.
- [16] K.K. Gupta and S. Jain (2014), Comprehensive review of a recently proposed multilevel inverter (2014), IET Power Electron., 7(3): 467-479.
- [17] Kiran T. S. et al., (2018), Pseudo Random Carrier Pulse Width Modulation scheme for the reduction of harmonic distortion for cascaded h-bridge modified multi level inverter, 9: 1-12.
- [18] Lai Y.-S., Chang Y.-T., Chen B.-Y., (2013), "Novel random-switching PWM technique with constant sampling frequency and constant inductor average current for digitally controlled converter," IEEE Trans. Ind. Electron., 60(8): 3126–3135.
- [19] A. Johny Renoald, M. S. Keerthana (2016) 'Design and Implementation of Super-Lift Multilevel Inverter using Renewable Photovoltaic Energy for AC Module Application, International Journal of Science Technology & Engineering, 2(11), 617-624.
- [20] Lim Y.-C., Wi S.-O., Kim J.-N., et al, (2010), "A pseudorandom carrier modulation scheme", IEEE Trans. Power Electron., 25(4): 797–805.
- [21] Lu S., Marieethoz S., Corzine K.A (2010) Asymmetrical cascade multilevel converters with no integer or dynamically changing dc voltage ratios: concepts and modulation techniques, IEEE Trans. Ind. Electron., 57(7): 2411–2418.
- [22] A. Johny Renoald, M. Dhivya (2017), Analysis on Super Lift Multilevel DC/AC Inverters using Photovoltaic Energy with AC Module Application, International Journal for Scientific Research & Development, 5(2), pp. 479-481.
- [23] Mathe L., Lungeanu F., Sera D., et al (2012) Spread spectrum modulation by using asymmetric-carrier random PWM. IEEE Trans. Ind. Electron., 59, (10): 3710–3718.
- [24] Mohammad Farhadi Kangarlu, Ebrahim Babaei and Mehran Sabahi, (2013), cascaded cross-switched multilevel inverter in 'symmetric and asymmetric conditions, IET Power Electronics, 6(6): 1041-1050.
- [25] Mohammad Najjar, Hossein Iman-Eini, Amirhossein Moeini, and Shahrokh Farhangi, (2017) Improving the Solution Range in Selective Harmonic Mitigation Pulse Width Modulation Technique for Cascaded Multilevel Converters, Journal of Power Electronics, 17(5): 1186-1194.
- [26] Mohammad Soltani, Hamidreza Pairo, Abbas Shoulaie, (2016) Modelling approach for multi-carrier-based pulse-width modulation techniques utilized in asymmetrical cascaded H-bridge inverters, 12(14):3822-3832.
- [27] Palanivel P & Dash SS (2011), Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques', IET Power Electronics, 4(8): 951-958.
- [28] Peyghambari A., Dastfan A., Ahmadyfard A, (2016) Selective voltage noise cancellation in three-phase inverter using random SV-PWM, IEEE Trans. Power Electron., 31(6): 4604–4612.
- [29] Shivam Prakash Gautam, Lalit Kumar Sahu, Shubhrata Gupta, (2016). Reduction in number of devices for symmetrical and asymmetrical multilevel inverters, IET Power Electronics, 9(4): 698-709.
- [30] Sivarani T. S., Joseph J. S., Agees K. C, (2016) Intensive random carrier pulse width modulation for induction motor drives based on hopping between discrete carrier frequencies, IET Power Electron., 9(3): 417–426.
- [31] A. Johny Renoald, V. Hemalatha, R. Punitha, M. Sasikala, M. Sasikala; (2016) Solar Roadways-The Future Rebuilding Infrastructure and Economy, International Journal of Electrical and Electronics Research, 4(2), pp: 14-19.
- [32] K. Santhiya, M. Devimuppudathi, D. Santhosh Kumar and A. Johny Renold, (2018), Real Time Speed Control of Three Phase Induction Motor by Using Lab View with Fuzzy Logic, Journal on Science Engineering and Technology, 5(2), pp.21-27.
- [33] Salman M., Haq I.U., Ahmad T. et al. Minimization of total harmonic distortions of cascaded H-bridge multilevel inverter by utilizing bio

- inspired AI algorithm. J Wireless Com Network, 66(1): 1-12.
<https://doi.org/10.1186/s13638-020-01686-5>.
- [34] A. Johny Renoald, M. Saranya, S. Shobana, R. Nivethitha; 'Patients Physical Condition Care Framework by Utilizing Web of Things (IoT), Journal of Control and Instrumentation Engineering, 6(1), pp.23-29. <http://doi.org/10.5281/zenodo.3773021>.
- [35] Vivek Kumar Gupta & Mahanty, R (2016) Optimized Switching Scheme of cascade H-bridge multilevel inverter using PSO International Journal of Electrical Power & Energy Systems, 64: 699-707.
- [36] Dhivya M. and A. J. Renoald. (2017) "Fuzzy Grammar Based Hybrid Split-Capacitors and Split Inductors Applied in Positive Output Luo-Converters." International journal of scientific research in science, engineering and technology 3, pp. 327-332.
- [37] Z. Du, L. M. Tolbert, B. Ozpineci and J. N. Chiasson, (2009), Fundamental Frequency Switching Strategies of a Seven-Level Hybrid cascaded H-Bridge Multilevel Inverter, IEEE Transactions on Power Electronics, 24 (1): 25-33.
- [38] Johny Renoald Albert, Saranya M, Shobana S; (2020) 'Drone based system for cleaning the environment, International Journal of Innovative Research in Science, Engineering and Technology, 9(3), pp. 1141-1145, DOI: 10.15680/IJRSET.2019.0903138.
- [39] A. Johny Renoald, D. Muhamadha Begam, B. Nishapriya (2021)," Micro grid connected solar PV employment using for battery energy storage system," Journal of Xidian University, 15(3): pp.85-97, <https://doi.org/10.37896/jxu15.3/010>.

Dr. Thenmalar K. (Namakkal, D. O. B: 29.06.1979). She received the B.E. degree in electrical and electronics engineering from Annamalai University, India in 2004, The Master Degree (M.E.) in the application of Power System from Annamalai University, India in 2011, and doctorate of philosophy (Ph.D.) in the application of Power system from Anna University Chennai, India in 2016. Currently she is working as an Associate

Professor/EEE department in Vivekanandha college of Engineering for Women, Tamilnadu, India.

Johny Renoald

He received the B.E. degree in electrical and electronics engineering from Anna University, Chennai, India, in 2009, The Master Degree (M.E.) in the application of Power electronics and drives from Anna University Coimbatore, India in 2012. The doctorate of philosophy (Ph.D.) in the application of Power electronics and drives from Anna University Chennai, India in 2021. His special field of interest

includes Power Systems and Power Electronics in Renewable Energy system. He was worked in Electrical Trainee in M.P.S STEELS PVT LTD., Kanjikode in the year of 2010, India. He joined the lecture/EEE in Erode Kongu polytechnic, Tamilnadu in the year of 2011-12. Currently he joined the department of Electrical and Electronics engineering, and currently is working as an Assistant Professor in Vivekanandha college of Engineering for Women, Tamilnadu, India.