

Delay Model Study of Single Ended Ring Oscillator (SERO)

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Abstract — In this study, a new general expression for the frequency of a SERO is constructed, which includes two additional variables, K_d and R_w , and improves upon the traditional equations by accounting for all analysis models and various width ratios. When compared with the the conventional equations, the proposed equation is a better alternate to study the frequency response when the width ratio is concerned parameter for researchers which is addressed by the variable R_w . A three stage SERO is simulated in 90 nm technology using Cadence Virtuoso platform to establish this equation. The value of K_d obtained remains almost equal which justifies the reason for using this approach traditionally to calculate the delay.

Keywords — frequency; propagation delay; single ended ring oscillator; voltage controlled oscillator.

I. INTRODUCTION

Voltage controlled oscillator (VCO) is an important element in the communication system and digital electronics for essential tasks such as frequency selection and clock signal generation [1,2]. Single ended ring oscillator (SERO) has been a popular choice for VCO over the inductor-capacitor (LC) oscillator because of its benefits in terms of simple manufacturability, smaller area and wider frequency tuning range [3]. A conventional SERO consists of an odd number of CMOS inverter stages as shown in Fig. 1. The load capacitances of each stage due to the MOSFET parasitics are also shown in Fig. 1.

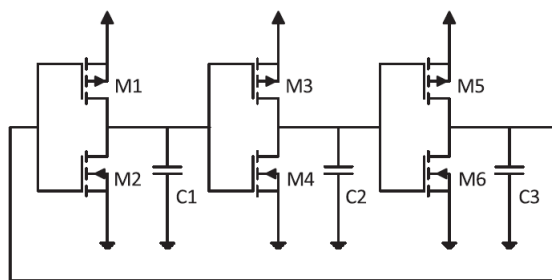


Fig. 1. Conventional SERO with load capacitances.

The expression of oscillating frequency in a RO is given by (1), which shows that the frequency is inversely proportional to the number of delay stages N and propagation delay t_{pd} at each stage [4]. The propagation delay t_{pd} is an average of the high-to-low and low-to-high propagation delays, t_{dHL} and t_{dLH} respectively [5]. Equation (1) can then be written as in (2).

$$f_{osc} = \frac{1}{2Nt_{pd}} \quad (1)$$

$$f_{osc} = \frac{1}{N(t_{dHL} + t_{dLH})} \quad (2)$$

Therefore, in order to analyze and estimate the frequency of oscillation, it is essential to correctly model the propagation delays t_{dHL} and t_{dLH} [6]. Two conventional methods exist to determine an approximate delay equation which analyze the CMOS inverter circuit differently. In the first method, the transistors are modelled as current sources with a constant current supply which charges and discharges the load capacitance C_L [7]. In the second method, the transistor is modeled as a resistor and an equivalent RC circuit is solved for the delay expression [8]. The point at which the delay is calculated can also vary and result in a similar equation with a different coefficient value. The propagation delay can be calculated when the output is at either 50%, 90% or 100% level of the supply voltage. Although the delay is calculated at the 50% level conventionally, as shown in Fig. 2, some equations mentioned in literature [9,10] have considered the 90% and 100% levels.

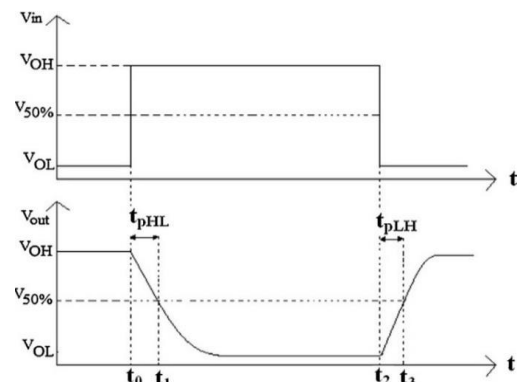


Fig. 2. Propagation delay calculation at 50% level.

These analyses can lead to 5 different frequency equations for a single circuit. Moreover, the equations are based on the assumption that the PMOS to NMOS width ratio, W_p/W_n is 2. The objective of this paper is to present the analytical derivations of all these 5 equations not available in literature and, hence, derive a new general expression for the frequency of an SERO which takes into account all analysis models and different width ratios. The rest of the paper is organized as follows: section II presents the derivation of the frequency equation based on different models, section III presents the proposed general expression and simulation results are presented in section IV. Finally, section V concludes the paper while providing insight to future scope.

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II. CONVENTIONAL FREQUENCY EQUATIONS

A. Current Source (CS) Model

1) Delay at 50% level

As mentioned before, one way to model the propagation delay is by assuming the transistors as current sources which charge and discharge the load capacitance. The charging and discharging current equations are then given by:

$$C_L \int_0^{\frac{V_{DD}}{2}} dV_{out} = \int_0^{t_{dLH}} I_p dt \quad (3)$$

$$C_L \int_{\frac{V_{DD}}{2}}^{V_{DD}} dV_{out} = - \int_0^{t_{dHL}} I_n dt \quad (4)$$

where, I_n and I_p are saturation currents of NMOS and PMOS transistors, respectively. The propagation delays t_{dLH} and t_{dHL} are obtained as (5) and (6). Assuming, $W_p/W_n = 2$ and, hence, $I_n = I_p = I_s$, the resultant frequency equation is obtained in (7), where I_s is the current through a single delay stage.

$$t_{dLH} = \frac{V_{DD} C_L}{2I_p} \quad (5)$$

$$t_{dHL} = \frac{V_{DD} C_L}{2I_n} \quad (6)$$

$$f_{osc} = \frac{I_s}{NV_{DD} C_L} \quad (7)$$

2) Delay at 90% level

For the delay calculation at 90% level, the integral limits are changed from $V_{DD}/2$ to $0.9V_{DD}$ and $0.1V_{DD}$ in equation (3) and (4), respectively. Equations (5) and (6) then change to equations (8) and (9). The resultant frequency then obtained is given by (10).

$$t_{dLH} = \frac{0.9V_{DD} C_L}{I_p} \quad (8)$$

$$t_{dHL} = \frac{0.9V_{DD} C_L}{I_n} \quad (9)$$

$$f_{osc} = \frac{I_s}{1.8NV_{DD} C_L} \quad (10)$$

3) Delay at 100% level

For the 100% level, the delay is calculated when the output reaches the voltage rails, V_{DD} or 0. In a similar method as before, the integral limits are now from 0 to V_{DD} and V_{DD} to 0 for equations (3) and (4), respectively. The propagation delays then obtained are given by (11) and (12) which leads to the frequency equation given by (13). This is the most common equation in literature.

$$t_{dLH} = \frac{V_{DD} C_L}{I_p} \quad (11)$$

$$t_{dHL} = \frac{V_{DD} C_L}{I_n} \quad (12)$$

$$f_{osc} = \frac{I_s}{2NV_{DD} C_L} \quad (13)$$

B. RC Model

As mentioned in section 1, the inverter can also be modelled as an RC network to obtain the propagation delay. Suppose, C_L is being charged to a voltage V_{out} from supply voltage V_{DD} when $V_{in} = 0$, as shown in Fig. 3. The operation of the network is described by the following differential equation [11]:

$$C_L \frac{dV_{out}}{dt} + \frac{V_{out} - V_{in}}{R_p} = 0 \quad (14)$$

where, R_p is the equivalent PMOS resistance. The output expression is given by (15).

$$V_{out} = \left(1 - e^{-\frac{t_{dLH}}{R_p C_L}}\right) V_{DD} \quad (15)$$

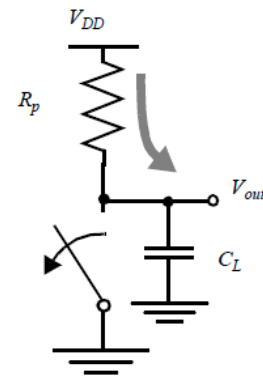


Fig. 3. RC model of CMOS inverter at $V_{in} = 0$.

1) Delay at 50% level

For calculating delay at 50% voltage level, $V_{out} = 0.5V_{DD}$ and the expression of t_{dLH} obtained is given by (16). Similarly for the discharging scenario, the expression of t_{dHL} is given by (17), where R_n is the equivalent NMOS resistance.

$$t_{dLH} = \ln(2) R_p C_L \quad (16)$$

$$t_{dHL} = \ln(2) R_n C_L \quad (17)$$

The average on-resistances R_n and R_p can be calculated by integrating the I-V characteristic curves of the NMOS and PMOS, respectively, over the interval of interest. For example, for 50% delay calculation, the expression of R_p is given by (18) where λ is the channel length modulation constant for short channel devices. Assuming $\lambda = 0$, the approximate expressions of R_p and R_n are given by (19) and (20).

$$R_p = \frac{1}{-\frac{V_{DD}}{2} \int_{V_{DD}}^{\frac{V_{DD}}{2}} \frac{VdV}{I_p(1 + \lambda V)}} \approx \frac{3V_{DD}}{4I_p} \left(1 - \frac{7}{9}\lambda V_{DD}\right) \quad (18)$$

$$R_p = \frac{3V_{DD}}{4I_p} \quad (19)$$

$$R_n = \frac{3V_{DD}}{4I_n} \quad (20)$$

Substituting equations (19) and (20) in (16) and (17), the resulting frequency equation is given by (21) where $I_s = I_n = I_p$, assuming $W_p/W_n = 2$.

$$f_{osc} = \frac{I_s}{1.5 \ln(2) N V_{DD} C_L} \quad (21)$$

2) Delay at 90% level

For calculating delay at 90% voltage level, $V_{out} = 0.9V_{DD}$ in equation (15) and the delay expressions obtained are given by (22) and (23).

$$t_{dLH} = \ln(10) R_p C_L \quad (22)$$

$$t_{dHL} = \ln(10) R_n C_L \quad (23)$$

The equivalent average on-resistances R_n and R_p are now calculated within the limits 0 and V_{DD} and the expressions are given by (24) and (25), respectively. Substituting (24) and (25) in (22) and (23), the resulting frequency expression obtain is given by (26).

$$R_n \approx \frac{V_{DD}}{I_n} \quad (24)$$

$$R_p \approx \frac{V_{DD}}{I_p} \quad (25)$$

$$f_{osc} = \frac{I_s}{2 \ln(10) N V_{DD} C_L} \quad (26)$$

Note that, using the RC model, the delay cannot be calculated at the 100% voltage level as the value of t_{dLH} from (15) evaluates to 0.

III. PROPOSED GENERAL EQUATION

The objective of this work is to present all 5 equations discussed above into one single equation while addressing the variable W_p/W_n ratio in the expression. Let $W_p = R_w W_n$, where R_w is the PMOS transistor to NMOS transistor width ratio. Since the frequency equations consist of the current I_s , a relation between I_n and I_p in terms R_w needs to be developed. Ideally when $R_w = 2$, $I_n = I_p = I_s$, and when $R_w = 1$, $I_n = 2I_p$. This is due to the difference in mobility of electrons and holes in NMOS and PMOS, respectively. Therefore, the relation between I_n and I_p is given by (27).

$$I_n = \frac{2}{R_w} I_p \quad (27)$$

Using this relation with the CS model and 50% delay calculation procedure, the high-to-low and low-to-high propagation delays obtained are given by:

$$t_{dHL} = \frac{C_L V_{DD}}{2I_p \frac{2}{R_w}} = \frac{R_w C_L V_{DD}}{4I_p} \quad (28)$$

$$t_{dLH} = \frac{C_L V_{DD}}{2I_p} \quad (29)$$

The summation of the two delays, t_d is given by equation (30).

$$t_d = t_{dHL} + t_{dLH} = \frac{2C_L V_{DD} + R_w C_L V_{DD}}{4I_p} \quad (30)$$

$$= \frac{C_L V_{DD} (1 + 0.5R_w)}{2I_p}$$

Using equation (30), the expression of oscillating frequency for the 50% CS model is given by (31) where, K_d is the coefficient of delay model and I_s is the source current. K_d is 0.5 in this case. Since, I_p is directly the current from the supply, I_p can be replaced with I_s .

$$f_{osc} = \frac{I_s}{K_d (1 + 0.5R_w) N C_L V_{DD}} \quad (31)$$

Similarly, the relation in (27) can be used for the remaining 4 models to obtain the same expression in (31) for the frequency but with different K_d value. The value of coefficient for the 5 different models are presented in Table I.

TABLE I: VALUE OF COEFFICIENT K_d FOR DIFFERENT MODELS

Model	K_d
50% CS	0.50
50% RC	0.52
90% CS	0.90
100% CS	1.00
90% RC	2.30

IV. SIMULATION RESULTS

A three stage SERO with load capacitances is simulated in 90 nm technology using Cadence Virtuoso platform. The supply voltage is varied between 0.3 V and 2 V. The value of the load capacitance is calculated using the equation in [12]. The circuit is first simulated with $R_w = 2$ and the new equation is compared with the conventional equations. The percentage of error between the proposed and existing equations for all values of V_{DD} , as given in Table II, shows that the proposed expression obtains the same result as the conventional equations when the width ratio is 2.

TABLE II: PERCENTAGE ERROR OF FREQUENCY

Model	50% CS	50% RC	90% CS	100% CS	90% RC
Error* (%)	0	-0.48	0	0	0

$$* Error = \frac{F_{new} - F_{conv}}{F_{conv}} \times 100$$

The circuit is re-simulated with $R_w = 0.33$ where $W_n = 360$ nm and $W_p = 120$ nm. The simulated frequency response is then compared with both conventional and proposed equation for all different models. The frequency-voltage characteristics shown in Fig. 4 proves that the proposed equation gives a better estimation (71% improvement) of the frequency since it addresses the changed width ratio.

V. CONCLUSIONS AND FUTURE SCOPES

The analytical frequency equation of an SERO can be obtained through various approaches leading to different results. The conventional methods also assume the ideal value of 2 for the PMOS to NMOS width ratio. A new general expression is proposed in this paper which introduces two new variables K_d and R_w . The value of K_d is given in Table 1 for different delay models which may be chosen for the frequency estimation. The variable R_w addresses the effect of

PMOS to NMOS width ratio on the frequency and provides 71% improvement than the conventional equations. Therefore, the proposed equation is a better alternate to the conventional equations to study the frequency response when the width ratio is concerned parameter for researchers. Using the 50% delay calculation for both CS and RC models, the value of K_d obtained remains almost equal which justifies the reason for using this approach traditionally to calculate the delay. In future, the effectiveness of the equation can be studied for more different width ratios and technologies. Although the proposed equation proves to be a better alternative, the percentage of errors with the simulated frequency response remain very high. This is because the current and load capacitance were assumed constant, though they are both voltage dependent. The MOSFETs' region of operation also changes during one voltage swing which changes the expressions of current and equivalent resistance. The current and load capacitance also need to be simulated

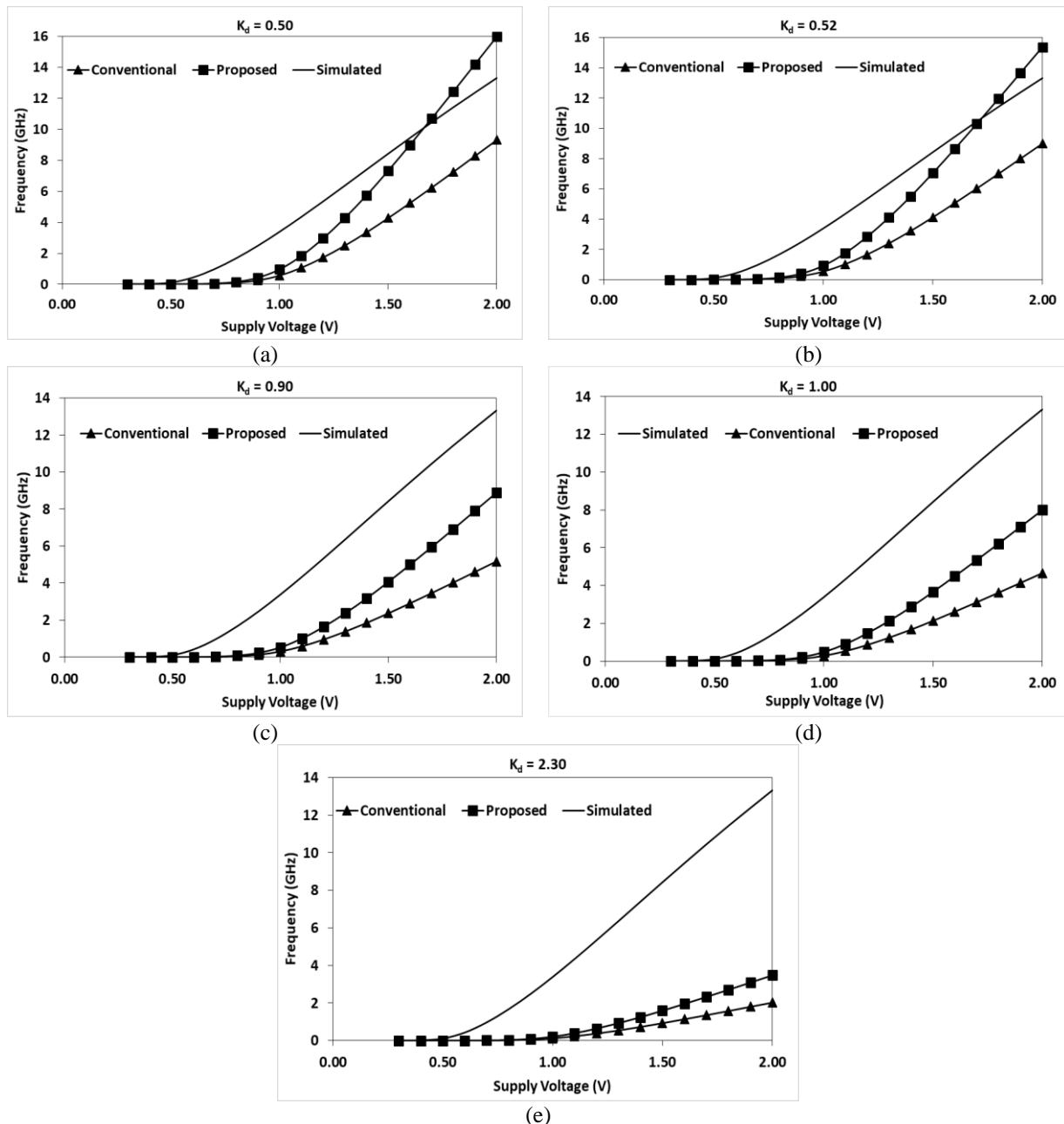


Fig. 4 Frequency-voltage characteristics for different models.

and calculated, respectively, to estimate the frequency which makes the equation futile for designers. A more accurate, while simple, frequency equation needs to be derived in future for reliable study of the RO frequency response.

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