Analysis of Decoupling Capacitor Performance in Improving Power Integrity in Two Layer/Three Layer Printed Circuit Boards

Rajesh Rehpade¹⁺, Gajanan Kharate¹, and Jayant Chopade³

ABSTRACT

Electronic circuits can only function properly if supplied with clean power. The clean power is only possible if the AC & D.C. noise in the power supply voltage which is supplied to electronic devices is below tolerance limits. To keep this noise within the limits, the impedance of Power Distribution Network (PDN) should be as minimal as possible. The use of Decoupling Capacitors is the most proven strategy to keep the PDN impedance low. In this paper, an attempt has been made to analyze the performance of PDN of a two-layer and three-layer P.C. Board, for the same set of Decoupling Capacitors. The PDN design has been carried out to meet an assumed set of specifications. The values of Interconnection Inductance have been obtained. The Interconnection Inductance is mostly responsible for PDN impedance, especially at higher frequencies. The simulations have been conducted for the PDN impedance of a two-layer as well as a three-layer P.C. Board. From the simulated impedance profiles, it is evident that PDN impedance obtained for a two-layer P.C. board is almost similar to that of a three-layer one if the width of the power supply trace is suitably tailored. It is therefore more prudent to go for a two-layer PDN configuration considering its simplicity and economy.

Keywords: Decoupling Capacitors, Interconnection Inductance, Power Distribution Network (PDN) Impedance, Printed Circuit (P.C.) Board.

1. INTRODUCTION

PCBs have been an essential part of every electronic system. The design of PCB layout has been limited only to rating of conductors and selecting their widths traditionally.

With Advent of high-speed semiconductor device, the speed of signals has increased considerably. To deliver these high-speed signals, the switching speed of Integrated Circuit has increased considerably [1]. These higher switching speeds coupled with higher magnitudes of load currents, induce noise in the Power Distribution Network (PDN).

The noise in the PDN Network severely affects the magnitude and shape of signals being delivered by Integrated Circuits. The PDN noise can only be minimized by reducing the value of PDN impedance. The reduction in PDN impedance is possible by increasing the width of power distribution network conductors. But, this traditional approach can no more work at high switching speeds. The use of decoupling capacitors for every high-speed IC is the only way to reduce the PDN impedance and make it noise-free. This paper discusses the performance of Decoupling capacitors, for improving Power Integrity [3] by reducing PDN impedance by selecting the value and number of Decoupling capacitors (Decaps) for keeping the PDN impedance below the targeted value over the entire frequency spectrum of circuit operation, in two layer and three layer Printed Circuit Board Configurations. To supplement the theoretical design approach, the design has been carried out for PDN system for delivery 1 A load current and switching speeds up to 1 GHz.

2. ROLE OF DECOUPLING CAPACITORS

Decoupling Capacitors (Decaps) are required to be connected to power supply pins of the semiconductor devices so as to meet instantaneous current demands thereby reducing power bus noise and hence improving the Power Integrity. Bulk capacitors play a major role in improving the performance of Power Distribution Network (PDN) at lower frequencies i.e., up to 1 MHz [3]. This can be
very easily done with one or two high value capacitors in
parallel connection. But the high-frequency performance
is the real challenging one. High-value capacitors are no
longer useful due to their sluggish response, therefore small
ceramic disc capacitors are required to be connected in
parallel. The parallel combination of several Decaps helps
in reducing ESL as well as ESR while increasing the total
equivalent capacitance.

3. Decoupling Capacitor Parasitics and their
Calculations

Equivalent series Inductance (ESL) of a Decap:

Total ESL of system = (ESL + Mounting Inductance
+ Spreading Inductance
+ Via Inductance)

3.1. The Basis for Calculations
1) Size of GND plane;
2) Size of PWR plane;
3) Distance of Decaps from IC;
4) Thickness of dielectric (Signal to GND);
5) Thickness of dielectric between GND & Power planes;
6) Decap specifications from manufacturer.

3.2. Assumptions
1. Length of power bus: 50 mm, width: 3.3 mm.
2. Distance of Decaps from IC power pins: 10 mm.
3. Dimensions of PWR and GND planes:
   • PWR plane = 50 × 50 mm
   • GND plane = 50 × 50 mm
4. Thickness of di-electric for FR-4 grade P.C.B lami-
nate: h = 1.5 mm.
5. Diameter of via: 0.305 mm.
6. The Decap specs: as mentioned in Table IV.

3.3. Calculation for a Two-Layer Board

Total ESL of Decap system = (ESLself + Parasitic interconnection inductance of Decaps)

Parasitic interconnection inductance of Decaps
= Spreading Inductance + Via Inductance

ESLself varies from capacitor to capacitor.

Circuit configuration (Two-layer) is depicted on Fig. 1.
Parasitic interconnection inductance of Decaps:
i) Via pair loop Inductance:

\[ L_{vp} \approx 0.4 \times h \times [\ln(2D/d) + 1/4] \text{nH} \] (1)

3.4. Calculation for a Three-Layer Board

Total ESL of Decap system = (ESLself + Parasitic interconnection inductance of Decaps)

Circuit configuration (Three-layer) is depicted on Fig. 2.
Parasitic interconnection inductance of Decaps:
ii) Spreading Inductance (loop inductance) of conductors from Decap to I.C.:

\[ L_{p-loop} = (1.28 h l/w) \text{nH} = 5.82 \text{nH} \] (3)

[5] The total Parasitic interconnection inductance of
Decaps:

\[ L_{ii} = L_{via} + L_{p-loop} = 6.49 \text{nH} \]

3.5. Calculation for a Two-Layer Board with Higher
Conductor Width

If the width of the conductor which connects Decap to
IC (W_{PWR}) is doubled, i.e., W_{PWR} = 2 × 3.2 = 6.6 mm,
then Parasitic interconnection inductance of Decaps in a
two-layer P.C. Board becomes:

\[ L_{via} \approx \text{remains unchanged i.e., 0.669 nH} \]

\[ L_{p-loop} = (1.28hl/w) \text{nH} = 2.91 \text{nH} \]

The total Parasitic interconnection inductance of
Decaps:

\[ L_{i} = L_{via} + L_{p-loop} = 0.669 + 2.9 = 3.57 \text{nH} \]
3. Analysis of Decoupling Capacitor Performance in Improving Power Integrity

Table I: Type of PC Board: Two Layer

<table>
<thead>
<tr>
<th>Dimensions (W x L) of power conductor connecting Decap to I.C.</th>
<th>Inductance of via or via pair of Decap, nH</th>
<th>Spreading inductance of conductors from Decap to I.C., nH</th>
<th>Total parasitic inductance to be added for Decaps, nH</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3 x 10 (Power Track)</td>
<td>0.669 (Via)</td>
<td>5.82</td>
<td>6.489</td>
</tr>
</tbody>
</table>

Table II: Type of PC Board: Three Layer

<table>
<thead>
<tr>
<th>Dimensions (W x L) of power conductor connecting Decap to I.C.</th>
<th>Inductance of via or via pair of Decap, nH</th>
<th>Spreading inductance of conductors from Decap to I.C., nH</th>
<th>Total parasitic inductance to be added for Decaps, nH</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 x 50 (Plane)</td>
<td>1.97 (Via pair)</td>
<td>4.4</td>
<td>6.37</td>
</tr>
</tbody>
</table>

Table III: Type of PC Boards: Two Layer with width Power Conductor Doubled

<table>
<thead>
<tr>
<th>Dimensions (W x L) of power conductor connecting Decap to I.C.</th>
<th>Inductance of via or via pair of Decap, nH</th>
<th>Spreading inductance of conductors from Decap to I.C., nH</th>
<th>Total parasitic inductance to be added for Decaps, nH</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.6 x 10 (Power Track)</td>
<td>0.669 (Via)</td>
<td>2.91</td>
<td>3.579</td>
</tr>
</tbody>
</table>

Table IV: Values of Decaps [6], [7]

<table>
<thead>
<tr>
<th>Capacitors</th>
<th>Capacitance nF</th>
<th>ESR mΩ</th>
<th>ESL nH</th>
<th>Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk</td>
<td>470000</td>
<td>4.5</td>
<td>1.35</td>
<td>2</td>
</tr>
<tr>
<td>Decap 1</td>
<td>47</td>
<td>40</td>
<td>0.86</td>
<td>10</td>
</tr>
<tr>
<td>Decap 2</td>
<td>0.049</td>
<td>25</td>
<td>0.79</td>
<td>9</td>
</tr>
<tr>
<td>Decap 3</td>
<td>0.680</td>
<td>320</td>
<td>0.3</td>
<td>8</td>
</tr>
</tbody>
</table>

3.6. Summary of Inductance Calculations

Inductance calculations have been summarized in Tables I–III.

4. Selection of Decoupling Capacitors

The following PDN Specifications were considered for the Design of PDN:

\[ V_{ss} = 3.3 \text{ V}, \quad I_{\text{max}} = 1 \text{ A}, \quad V_{\text{ripple}} = 5.5\% \]

Bandwidth (Highest frequency) = 1 GHz.

Decoupling capacitors were selected for achieving the target impedance, \( Z_{T-PDN} \).

\[ Z_{T-PDN} \leq [(V_{ss} \times \text{Ripple %})/0.5 I_{\text{max}}] \leq 0.363 \Omega \]

[5], [9] PDN was designed to meet above specifications using Frequency Domain Target impedance method [10], [11]. The Decaps were selected and the values of their parasitics such as ESR, ESL were obtained from manufacturer’s data sheets [6], [12]. These values are mentioned in Table IV.

5. Simulation Results

PDN Impedance Profile for a 2-Layer P.C. Board [13] with Higher Width of Conductor from Decap to I.C. for Decaps Listed in Table IV is shown in Fig. 3.
PDN Impedance Profile for a 3-Layer P.C. Board with set of Decaps Listed in Table IV is shown in Fig. 4. PDN Impedance Profiles for a 3-Layer and 2-Layer P.C. Boards with the set of Decaps Listed in Table IV is shown in Fig. 5.

6. Conclusion

Power Integrity is absolutely essential for high speed printed circuit boards. It can be achieved only if the impedance of conductors which are part of the power distribution system is kept low. The low impedance of the Power Distribution Network can be realized by using decoupling capacitors of specific values and quantities. A three-layer P.C. Board has dedicated layers for power and ground planes. The impedance profile obtained for a three-layer P.C. Board for a set of values and quantity of Decoupling Capacitors has shown a maximum impedance of 0.338 Ω, at the highest frequency of 1 GHz. Whereas a two-layer P.C. Board with one layer as a Ground plane and the other for power/signal conductors, when simulated for the same set of decoupling capacitors, the PDN impedance at 1 GHz, was found to be, 0.336 Ω. The reduction is possible as Two two-layer configuration has a lesser number of vias than that of a Three-layer P.C. Board. It can therefore be concluded that better performance can be obtained from a PDN of a two-layer P.C. Board if the width of the power conductor is tailored beyond theoretical design values obtained for carrying the specified load current. Thus, it shall be more economical and simpler, if a two-layer P.C. Board is preferred over a three-layer, at higher frequencies, in particular.

References